

An Autocalibrated CMOS Bandgap Reference with Improved PVT Robustness in 65 nm CMOS Technology

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Abstract – This paper presents a precision CMOS bandgap reference with an integrated autocalibration mechanism, implemented in the TSMC 65 nm GP process. The circuit operates from dual supply voltages of 1.8 V for analog and 1.2 V for digital domains, consuming 1.064 mW across the temperature range of $-40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ and occupying area of 0.066 mm^2 . It provides a $1.2265\text{ V} \pm 8.5\text{ mV}$ (3σ) bandgap output, a 1 V reference, and proportional-to-absolute-temperature (PTAT) and zero-temperature-coefficient (ZTAT) reference currents. The autocalibration algorithm adjusts internal PTAT currents using an external precision resistor as a calibration standard, effectively compensating for process variations without manual trimming. Simulation results demonstrate high stability, low temperature dependence, and improved process robustness, making the circuit suitable for high precision mixed-signal systems-on-chip applications.

Keywords – bandgap reference, CMOS, process variation compensation, autocalibration, analog CMOS design, TSMC 65nm technology.

I. INTRODUCTION

Precision voltage references are essential building blocks in mixed-signal and analog integrated systems such as ADCs, DACs, and power management units. Their accuracy and stability directly affect the overall system performance.

Conventional bandgap reference circuits, although well established, suffer from performance degradation caused by process, voltage, and temperature (PVT) variations. Furthermore, fine trimming after fabrication is often required to achieve the desired precision, increasing test cost and complexity.

This work presents a CMOS bandgap reference with autocalibration designed in the TSMC 65 nm GP process. The circuit combines a classical bandgap core with a digital calibration circuit that automatically compensates for process-induced variations using an external precise resistor. This approach eliminates the need for manual trimming.

II. BACKGROUND AND THEORY

Bandgap reference circuits generate a temperature-independent voltage V_{BG} by summing two temperature-dependent terms: a complementary-to-absolute-temperature (CTAT) component, the base-emitter voltage V_{BE} of a bipolar transistor, and a proportional-to-absolute-

temperature (PTAT) voltage derived from the difference of two base-emitter voltages ΔV_{BE} biased at different current densities.

$$V_{BG} = V_{BE} + K \cdot \Delta V_{BE} = V_{BE} + K \cdot V_T \ln(n) \quad (1)$$

Where $V_T = kT/q$ is the thermal voltage and K is set to such a ratio that results in the smallest temperature coefficient of V_{BG} .

As a byproduct of generating this reference voltage a PTAT type current is generated in the circuit. This type of current is frequently used as a bias current for many on chip circuits in order to compensate for the performance degradation due to temperature variations.

The proposed design extends the classical topology by introducing an autocalibration loop capable of digitally correcting resistor and current mismatches through controlled current scaling. This achieves consistent output precision across PVT variations without requiring post-fabrication trimming.

III. SYSTEM ARCHITECTURE

A simplified block diagram of the system is shown in Fig. 1.

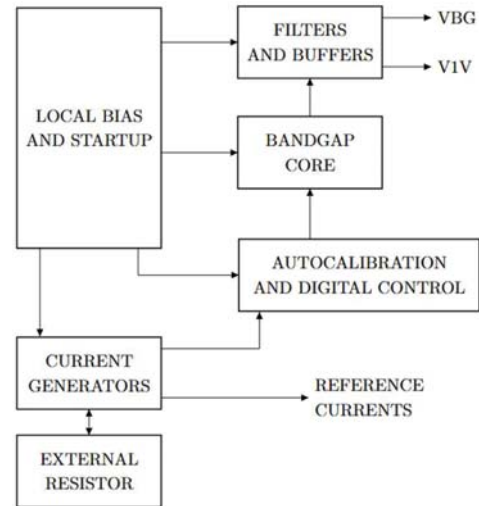


Fig. 1. Simplified system block diagram

At the heart of the design lies the bandgap core, which generates the primary temperature-independent reference

An embedded autocalibration controller manages on-chip calibration by comparing internally generated references against an external precision resistor, REXT. Through this mechanism, the circuit compensates process-induced deviations in the PTAT currents.

A startup detection circuit has also been implemented and a digital signal BGOK is used to represent when the bandgap core has successfully started up.

For a faster startup time filter caps used for improving

The final layout occupies 65941 μm^2 (271 $\mu\text{m} \times 244 \mu\text{m}$). Block placement was optimized to minimize parasitics and reduce coupling of critical lines.

Fig. 4. Simplified schematic of the comparator circuit

The autocalibration circuit compares internal PTAT and ZTAT currents. This is performed by a voltage comparator that compares voltage drops across the same on-chip resistors that are driven by PTAT and ZTAT currents. A digital state machine iteratively adjusts the 6-bit trim register controlling PTAT currents until the desired current levels are achieved. Once calibration completes, the system operates autonomously without further adjustment. This calibration is to be performed at room temperature of 27 °C.

Calibration is initiated with a rising edge of the TRIM_START signal if the RESET signal is high. If necessary, the circuit waits for the core to successfully turn on which is indicated with the internal BGOK signal. After the registers have been setup the main calibration loop is started. A counter is being incremented at every rising edge of the clock signal and the output of the comparator is checked on every falling edge. This cycle continues until the comparator output COMP_OUT is high, at which point the calibration is complete and this is indicated with a high value of TRIM_COMPLETE signal. Proper calibration code that has been found is written in the calibration code register inside the reference. This code can be accessed from the outside of the reference if there is a need to store it elsewhere, presumably in a non-volatile memory.

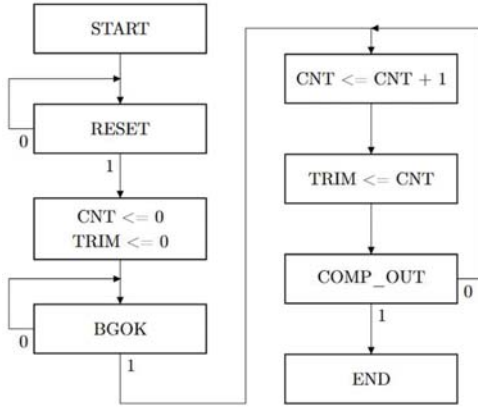


Fig. 5. Simplified autocalibration flow diagram

VI. SIMULATION RESULTS

Post-layout simulations were performed across PVT corners and Monte Carlo (MC) variations in nominal operating conditions (100 samples). The key results after trimming across PVT and MC in typical conditions are summarized in Table I and II, respectively.

Performance comparison with similar circuits is shown in Table III. The circuit presented in this paper when compared to them has a better reference voltage temperature coefficient and shows comparable σ . PSRR has a larger bandwidth, but its' value at DC is lower. Power dissipation is higher than other circuits and this is the result of higher PSRR bandwidth as well as due to having the reference voltages buffered. Device sizes are also larger, and they

consume more power in order to reduce mismatch.

TABLE I
SUMMARY OF KEY SIMULATION RESULTS ACROSS PVT.

Parameter	Simulation values		
	Minimum	Nominal	Maximum
VBG [V]	1.218	1.227	1.235
V1V [V]	0.9943	1.002	1.009
IPTAT [μ a]	9.961	10.020	10.080
TC IPTAT [$m/^{\circ}C$]	7.202	7.473	7.710
ICONST [μ A]	9.984	10.050	10.080
IOFF [nA]	16.81	349	21460
ION [μ A]	250.3	313.8	540.6
t START [μ s]	4.516	8.475	14.56
PSRR@1kHz [dB]	40.96	55.73	58.59
PSRR@10kHz [dB]	37.83	40.77	43.12
PSRR@100kHz [dB]	32.22	34.23	35.08
PSRR@1MHz [dB]	31.82	33.2	35.38
Noise@1kHz [μ V/ $\sqrt{Hz}$]	2.640	3.067	3.580
Noise RMS [μ V]	183	208	240

TABLE II
SUMMARY OF KEY SIMULATION RESULTS ACROSS MC IN TYPICAL CONDITIONS.

Parameter	Simulation values		
	Minimum	Mean	Maximum
VBG [V]	1.220	1.227	1.235
V1V [V]	0.9943	1.002	1.009
IPTAT [μ a]	9.961	10.020	10.080
TC IPTAT [$m/^{\circ}C$]	7.350	7.473	7.640
ICONST [μ A]	9.917	9.989	10.060
IOFF [nA]	127.5	515.1	1611
ION [μ A]	280.7	356.7	421.3
t START [μ s]	7.286	8.479	9.830
PSRR@1kHz [dB]	55.29	55.71	56.03
PSRR@10kHz [dB]	39.95	40.78	41.61
PSRR@100kHz [dB]	32.91	34.22	34.4
PSRR@1MHz [dB]	32.72	33.18	33.66

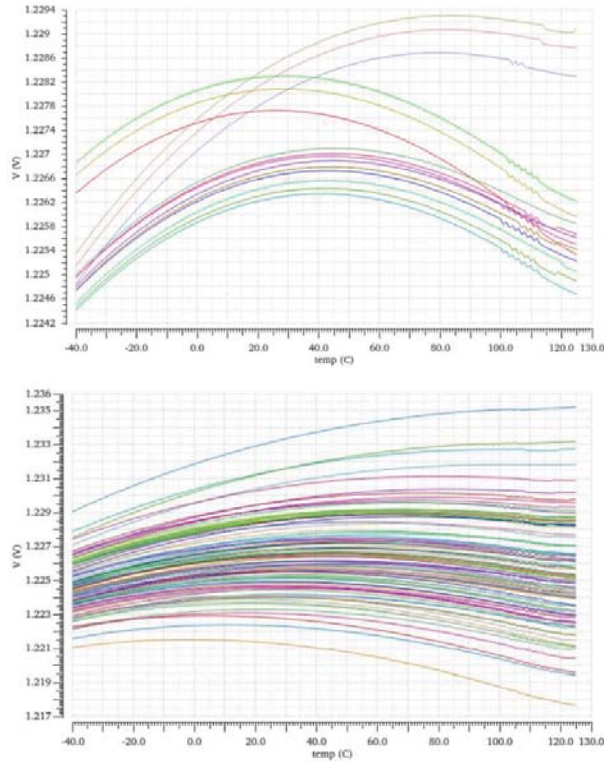


Fig. 6. Simulated VBG versus temperature across PVT (top) and MC (bottom)

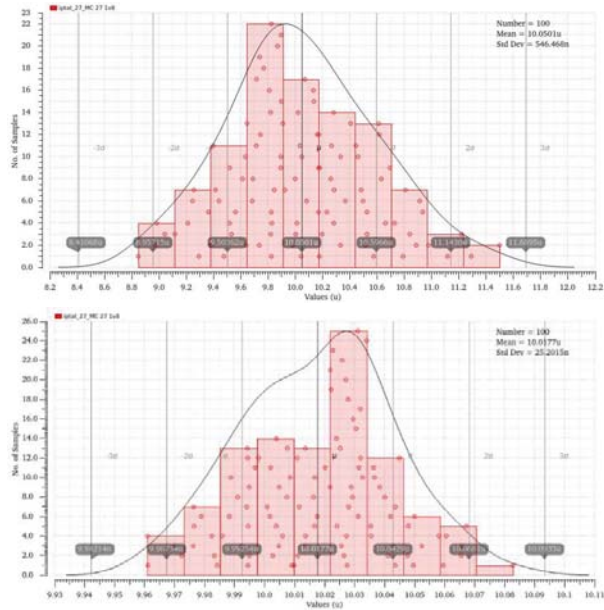


Fig. 7. Monte Carlo histogram of nominal PTAT current value before (top) and after trimming (bottom).

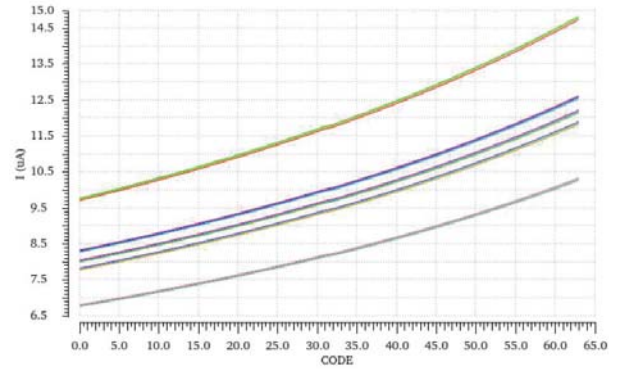


Fig. 8. Nominal value of IPTAT versus trim code across process and voltage variations

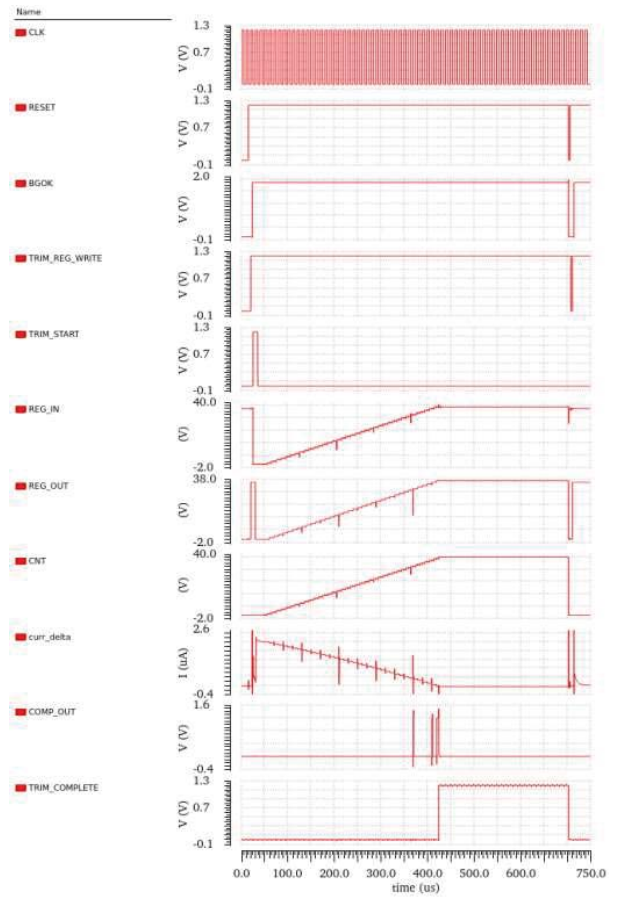


Fig. 9. Transient waveforms of different signals during the autocalibration process in typical condition

TABLE III
PERFORMANCE COMPARISON WITH SIMILAR CIRCUITS.

Parameter	This work	[9]	[10]	[11]	[12]	[13]
CMOS node	65 nm	65 nm	90 nm	0.6 μm	0.4 μm	65 nm
Supply Voltage [V]	1.8	1.2	0.6	0.98	0.84	1.2 – 2.5
Power [μW]	1064	-	547	17.6	4.6	0.972
Reference Voltage @ 27 °C [V]	1.227	0.467	0.243	0.603	518	1.0011
Reference Voltage TC [ppm/°C]	10.05	30.9	150	15	116	22.3
Reference Voltage σ [mV]	2.83	-	-	-	5.06	1.2
Temperature Range [°C]	-40 to 125	-55 to 125	5 to 100	0 to 100	27 to 125	-40 to 120
PSRR [dB]	40.96 @ 1 kHz	61 @ DC	-	44 @ 100 Hz	65 @ DC	58 @ DC
Area [mm ²]	0.066	0.5025 (including bondpads)	0.0319 (approximate)	0.24	0.1	0.04

VI. CONCLUSION

A CMOS bandgap reference with autocalibration has been designed and verified in the TSMC 65 nm GP process. The circuit operates from 1.8 V/1.2 V dual supplies, consumes 1.064 mW, and achieves a 1.2265 V reference with ± 8.5 mV (3σ) variation across -40 °C to 125 °C.

The digital calibration loop effectively compensates process-induced mismatches, enhancing precision without post-fabrication trimming. Future work includes improving the existing calibration circuit by moving it outside of the bandgap core and adding low-dropout (LDO) regulators to reduce the load dependence of the reference voltage generators.

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